ABSTRACT

0034 A shallow trench isolation (STI) structure and method of forming the same with reduced stress to improve charge mobility the method including providing a semiconductor substrate comprising at least one patterned hardmask layer overlying the semiconductor substrate; dry etching a trench in the semiconductor substrate according to the at least one patterned hardmask layer; forming one or more liner layers to line the trench selected from the group consisting of silicon dioxide, silicon nitride, and silicon oxynitride; forming one or more layers of trench filling material comprising silicon dioxide to backfill the trench; carrying out at least one thermal annealing step to relax accumulated stress in the trench filling material; carrying out at least one of a CMP and dry etch process to remove excess trench filling material above the trench level; and, removing the at least one patterned hardmask layer.